REMARKS

Claims 1-24 and 28-29 remain pending in the current Application. Claims 23 and 28 have been amended; and claims 25-27 have been cancelled. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Drawings

Applicants are submitting a replacement sheet for FIG. 2 to address the Examiner's objection. In FIG. 2, Applicants have removed the arrow from the output of element 50 because it is not necessary. That is, block 50 of FIG. 2 includes "Output best cell layout" which is the end of the illustrated flow diagram. Therefore, Applicants request that the Drawings be accepted by the Examiner.

Specification

Applicants have amended the title to "Method for Automated Transistor Folding," as suggested by the Examiner.

Respecting Examiner's request that Applicants include a *Summary of Invention*, Applicants respectfully point out that (1) 37 CFR 1.77(b) states "The specification *should* include the following sections in order: [(b)(1) through (b)(11)]," (wherein (b)(6) is Brief Summary of the Invention); and (2) both 37 CFR 1.73 and the MPEP 608.01(d) state, "Such summary [of the Invention] should, *when set forth* be commensurate with the invention as claimed and any object recited should be that of the invention as claimed." Applicants accordingly submit that both Title 37 of the Code of Federal Regulations (CFR) and the Manual of Patent Examining Procedure (MPEP) unambiguously state, by using the word *should* and not

must, that the Brief Summary of the Invention is optional with respect to its use in U.S. Patent Applications. Accordingly, because Federal Law does not so require, Applicants choose not to include a Summary of the Invention in the current Application.

Objection to claim 15

Applicants have amended claim 15 to correct a typographical error. Claim 15 now depends from claim 14 rather than itself.

Rejection of claims 1-3, 14-18, and 23-26 under 35 U.S.C. 103(a)

Applicant respectfully submits that claims 1-3, 14-18, and 23-26 are patentable over US Patent No. 5,995,734 (hereinafter referred to as Saika).

With respect to claim 1, Applicants submit that claim 1 is not taught or suggested by Saika because Saika does not teach or suggest each and every element of claim 1. For example, claim 1 includes determining that more than one of the plurality of transistors are the widest transistors and that the more than one widest transistors all have the same width, folding only one of the widest transistors to produce a folded transistor, and creating a fold solution for the layout with the one folded transistor. The Examiner specifically points to figures 16(a) and (b) of Saika to point out that the transistors trc and trd (P-channel) and trg and trh (N-channel) are widest transistors which are folded to form trc1, trc2, trd1, trd2, trg1, trg2, trh1, and trh2, respectively. However, note that *all* widest transistors are folded at once to create a transistor placement. That is, Saika does not teach or suggest folding only one of the widest transistors to produce a folded transistor. Furthermore, the Examiner agrees that Saika does not specifically teach a folding solution as claimed in claim 1, but proceeds to state that Saika teaches "a method of determining which transistor needs to be folded based on predetermined height value of cell and wiring density, and then made decision of folding." However, as pointed out above, Saika never teaches or even suggest creating any type of folding solution using the one folded transistor, as claimed in claim 1. Instead, Saika only teaches a solution in which all transistors are folded at once. Furthermore, one would not be motivated to fold only one transistor in Saika because the placement process of Saika would no longer operate as intended. Therefore, for at

least those reasons given above, the Examiner has failed to make a prima facie case of obviousness with respect to claim 1.

Claims 2-8 have not been independently addressed because they depend directly or indirectly from allowable claim 1, and are therefore allowable for at least those reasons stated above with respect to claim 1.

With respect to claim 14, Applicants submit that claim 14 is not taught or suggested by Saika because Saika does not teach or suggest each and every element of claim 14. For example, claim 14 includes iteratively folding only one transistor at a time of the plurality of transistors that have a width greater than a predetermined width to produce two transistors, and after each iteration, creating a fold solution after each iteration and adding the fold solution to a fold solution list. As with claim 1, the Examiner specifically points to figures 16(a) and (b) of Saika to point out that the transistors trc and trd (P-channel) and trg and trh (N-channel) are widest transistors which are folded to form trc1, trc2, trd1, trd2, trg1, trg2, trh1, and trh2, respectively. However, in Saika, note that all widest transistors are folded at once to create a transistor placement. Furthermore, the Examiner agrees that Saika does not specifically teach creating a folding solution as claimed in claim 14, but proceeds to state that Saika teaches "a method of determining which transistor needs to be folded based on predetermined height value of cell and wiring density, and then made decision of folding." However, Saika does not teach or suggest iteratively folding only one transistor at a time and creating a fold solution after each iteration. Furthermore, one would not be motivated to fold only one transistor at a time in Saika because the placement process would become too time consuming and would not operate as intended. Therefore, for at least those reasons given above, the Examiner has failed to make a prima facie case of obviousness with respect to claim 14.

Claims 15-22 have not been independently addressed because they depend directly or indirectly from allowable claim 14, and are therefore allowable for at least those reasons stated above with respect to claim 14.

With respect to claim 23, Applicants submit that Saika does not teach or suggest each and every element of claim 23. However, in order to further prosecution and not for prior art reasons, Applicants have amended claim 23 to include allowable claim 27 and any intervening claims. Applicants have cancelled claims 25-27 and have also amended claim 28 to depend from claim 23 rather than cancelled claim 27.

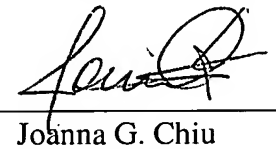
Conclusion

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action since reasons for the patentability of each pending claim is provided without addressing these statements. However, Applicants reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,



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SEND CORRESPONDENCE TO:

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